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(54) Spread spectrum clock generator and associated method.

(57) A clock circuit includes an oscillator (15) for generating a reference frequency signal, and a spread spectrum clock generator (14) cooperating with the oscillator for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency. The spread spectrum clock generator preferably includes a clock pulse generator for generating a series of clock pulses, and a spread spectrum modulator for frequency modulating the clock pulse generator to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced by the clock pulse generator. The spread spectrum modulator frequency modulates the clock pulses with specific profiles of frequency deviation versus the period of the profile. Electronic devices including the spread spectrum clock circuit and associated method are also disclosed.

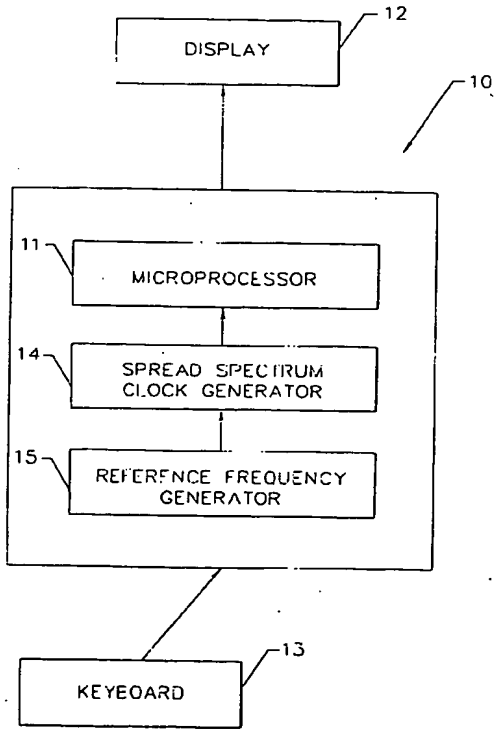

FIG. 1.

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a series of clock pulses, and spread spectrum modulating means for modulating the clock pulse generating means to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced by the clock pulse generating means.

The clock pulse generating means, if unmodulated, would typically produce generally rectangular or trapezoidal electrical pulses which, in turn, would generate corresponding impulse-shaped EMI spectral components at harmonics of the fundamental frequency. The spread spectrum modulating means reduces the peak amplitude of the EMI spectral components that would otherwise be produced. Accordingly, expensive shielding or other EMI suppression techniques may be reduced or eliminated in an electronic device including the spread spectrum clock generating circuit of the present invention. As would be readily understood by those skilled in the art, the spread spectrum clock generating circuit may find wide application in a number of electronic devices, particularly those including a microprocessor or microcontroller, such as a personal computer.

The spread spectrum modulating means preferably includes frequency modulating means for frequency modulating the clock pulse generating means. The frequency modulating means, in turn, preferably includes profile modulating means for frequency modulating the clock pulse generating means with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period. Several preferred or effective ranges for such modulating periodic waveforms are described later herein. In general, the preferred waveforms are more complicated than a simple sine wave in order to thereby reduce the spectral peak of EMI components by broadening and flattening their shape.

The clock pulse generating means preferably includes a phase locked loop as is commonly used in a conventional clock generating circuit. The frequency modulation means may be implemented by several types of circuits including an analog modulating generator or a programmable modulating generator which can produce a predetermined profile for the frequency deviation. In addition, the frequency modulating means is preferably capable of modulating the clock pulse generating means with a periodic waveform having a period of less than about 500 microseconds, that is, the frequency of modulation is desirably greater than about 2 KHz.

A method according to the invention is for generating a clock output signal with reduced amplitude EMI spectral components. The method includes the step of generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency. The step of generating a spread spectrum clock output signal preferably includes the steps of generating a series of clock pulses, and spread spectrum modulating the series of clock pulses to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced along with the series of clock pulses. The step of spread spectrum modulating the series of clock pulses preferably includes the step of frequency modulating the clock pulses with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period.

Embodiments of the invention will now be described by way of example only and with reference to the accompanying drawings, in which:

FIG. 1 is a schematic block diagram of a personal computer including a spread spectrum clock generating circuit in accordance with the invention.

FIG. 2 is a graph illustrating a reduction of peak spectral amplitude of a harmonic of the clock fundamental frequency produced by the spread spectrum clock generating circuit in accordance with the present invention.

FIG. 3 is a graph illustrating an embodiment of a desired modulation profile for producing a spread spectrum modulated clock signal in accordance with the present invention.

FIG. 4 is a graph illustrating several modulation profile ranges for producing a spread spectrum modulated clock output signal in accordance with the present invention.

FIG. 5 is a graph illustrating yet another embodiment of a desired modulation profile for producing a spread spectrum modulated clock output signal in accordance with the present invention.

FIG. 6 is a schematic block diagram illustrating a first circuit embodiment for producing the spread spectrum modulated clock output signal in accordance with the present invention.

FIG. 7 is a schematic block diagram illustrating a second circuit embodiment for producing the spread spectrum modulated clock output signal in accordance with the present invention.

FIG. 8 is a schematic block diagram illustrating a third circuit embodiment for producing the spread spectrum modulated clock output signal in accordance with the present invention.

FIG. 9 is a schematic block diagram illustrating a fourth circuit embodiment for producing the spread spectrum modulated clock output signal in accordance with the present invention.

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, applicants provide these embodiments so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

Referring first to FIGS. 1 through 5, an electronic device incorporating the spread spectrum clock generating circuit and its basic operation are first explained. As shown in FIG. 1, an electronic device, such as the schematically illustrated personal computer **10**, may benefit by having reduced measurable EMI spectral component emissions provided by the spread spectrum clock generator **14** (SSCG) according to the invention. A reference frequency generator **15**, such as a piezoelectric crystal driven at its resonant frequency by a suitable driver or oscillator circuit, provides a reference frequency for the SSCG **14**. The illustrated personal computer **10** also includes a display **12** and a keyboard **13**.

As would be readily understood by those of skill in the art, a number of electronic device incorporating microprocessors or other digital circuits requiring a clock signal for synchronization may also desirably incorporate the SSCG **14**. For example, computer printers may also desirably include the SSCG **14**.

The SSCG **14** generates the spread spectrum output clock signal by frequency modulating a typical clock signal including a series of trapezoidal or generally rectangularly-shaped electrical clock pulses. The modulation reduces the spectral amplitude of the EMI components at each harmonic of the clock when compared to the spectrum of the same clocking signal without modulation. FIG. 2 is a schematic representation of this effect where the spectral amplitude versus frequency at a harmonic (NF) is indicated by the plot labelled **M**. As also shown, the spectrum at the same harmonic of a standard clock signal is given as an impulse function labelled **I**. The spectrum of the SSCG output clock signal at the same harmonic ideally assumes a trapezoidal shape as illustrated by the plot labelled **T**.

Although in general the spectral "width" of the spread spectrum output clock signal at a harmonic is greater than the width of the standard non-modulated clock signal, the maximum amplitude for the harmonic is reduced. In an actual implementation, the amplitude of the spread spectrum modulated harmonic will not be uniform, but will exhibit some peaking near the center frequency and at the edges as illustrated by the plot **M**.

In order to minimize the amplitude of the signal for all frequencies, the modulation of the standard clock signal must be uniquely specified. Accordingly, the SSCG **14** includes profile modulating means for frequency modulating the clock pulse generating means with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period. The modulation profiles described herein produce relatively optimized flat spectral amplitudes at each harmonic. In general, the preferred profiles are more complicated than a simple sine wave in order to thereby reduce the measurable spectral peaks of the EMI components. Stated in other terms, the present invention converts narrow band harmonics into broadband signals that significantly reduce the measured emissions for the FCC and other regulatory bodies worldwide. These emission reductions may permit corresponding cost reductions of about $20 or more per product, as compared to the cost of conventional measures to suppress or shield EMI emissions.

FIG. 3 illustrates a typical profile of the frequency deviation versus time as may be used within the SSCG **14**. The maximum deviation illustrated is 100 KHz. This maximum frequency deviation is desirably programmable via a serial link with an upper limit of the maximum deviation being preferably about 250 KHz for typical current applications. However, depending on the application, the maximum deviation may be much greater than 250 KHz as would be readily understood by those skilled in the art. As would be also readily understood by those skilled in the art, a standard, non-modulated clock signal may be obtained by programming the maximum deviation to 0.

The frequency of the signal modulating the profile shown in FIG. 3 is 30 KHz. Significant peak amplitude reduction may also be achieved where the frequency is above 2 KHz, that is, where the period of the modulating waveform or profile is less than about 500 µsec. This frequency is also desirably programmable via the serial link or may be fixed dependent on the application. The modulating profile illustrated is a linear combination of a standard triangular wave and its cubic. The values of the profile are given in TABLE 1 below for maximum frequency deviations of 100 KHz and 200 KHz. For maximum deviations other than 100 KHz or 200 KHz, values for the modulating signal can be obtained by simply scaling the values found in TABLE 1 as would be readily appreciated by those skilled in the art.

Time (μS)	Deviation (KHz) 100 KHz Maximum	Deviation (KHz) 200 KHz Maximum
0	-100	-200
0.520833	-88.4615	-176.923
1.041667	-76.9231	-153.846
1.5625	-67.3077	-134.615
2.083333	-59.6154	-119.231
2.604167	-51.9231	-103.846
3.125	-44.2308	-88.4615
3.645833	-38.4615	-76.9231
4.166667	-32.6923	-65.3846
4.6875	-26.9231	-53.8462
5.208333	-23.0769	-46.1538
5.729167	-19.2308	-38.4615
6.25	-13.4615	-26.9231
6.770833	-9.61538	-19.2308
7.291667	-7.69231	-15.3846
7.8125	-3.84615	-7.69231
8.333333	0	0
8.854167	3.846154	7.692308
9.375	7.692308	15.38462
9.895833	9.615385	19.23077
10.41667	13.46154	26.92308
10.9375	19.23077	38.46154
11.45833	23.07692	46.15385
11.97917	26.92308	53.84615
12.5	32.69231	65.38462
13.02083	38.46154	76.92308
13.54167	44.23077	88.46154
14.0625	51.92308	103.8462

TABLE 1.
Frequency deviation values for maximum frequency deviations of 100 KHz and 200 KHz with a modulating frequency of 30 KHz.

Time (μS)	Deviation (KHz) 100 KHz Maximum	Deviation (KHz) 200 KHz Maximum
14.58333	59.61538	119.2308
15.10417	67.30769	134.6154
15.625	76.92308	153.8462
16.14583	88.46154	176.9231
16.66667	98.07692	196.1538
17.1875	88.46154	176.9231
17.70833	76.92308	153.8462
18.22917	67.30769	134.6154
18.75	59.61538	119.2308
19.27083	51.92308	103.8462
19.79167	44.23077	88.46154
20.3125	38.46154	76.92308
20.83333	32.69231	65.38462
21.35417	26.92308	53.84615
21.875	23.07692	46.15385
22.39583	19.23077	38.46154
22.91667	13.46154	26.92308
23.4375	9.615385	19.23077
23.95833	7.692308	15.38462
24.47917	3.846154	7.692308
25	0	0
25.52083	-3.84615	-7.69231
26.04167	-7.69231	-15.3846
26.5625	-9.61538	-19.2308
27.08333	-13.4615	-26.9231
27.60417	-19.2308	-38.4615
28.125	-23.0769	-46.1538
28.64583	-26.9231	-53.8462

TABLE 1. - Continued
Frequency deviation values for maximum frequency deviations of 100 KHz and 200 KHz with a modulating frequency of 30 KHz.

Time (μS)	Deviation (KHz) 100 KHz Maximum	Deviation (KHz) 200 KHz Maximum
29.16667	-32.6923	-65.3846
29.6875	-38.4615	-76.9231
30.20833	-44.2308	-88.4615
30.72917	-51.9231	-103.846
31.25	-59.6154	-119.231
31.77083	-67.3077	-134.615
32.29167	-76.9231	-153.846
32.8125	-88.4615	-176.923
33.33333	-100	-200

TABLE 1. - Continued
Frequency deviation values for maximum frequency deviations of 100 KHz and 200 KHz with a modulating frequency of 30 KHz.

Referring now more particularly to FIG. 4, several preferred ranges of profiles of frequency deviation are illustrated. In particular, the profiles are expressed as a percentage of frequency deviation versus a percentage of the period (% Period) of the periodic waveform. The outermost range or envelope is illustrated by the dotted lines labelled F_1, F_2 in the second quadrant II, that is, between 0% and 25% of the period. Straightforward symmetry defines the boundaries in the other indicated quadrants as described. Accordingly, those of skill in the art may readily implement and scale the ranges for a desired application.

The dotted lines may be defined mathematically by predetermined upper and lower bounds for the second quadrant II. The upper bound F_1 is defined by

$$100\%\left[-1+\sqrt{-\left(\frac{\%\ Period}{25}\right)^2+4\left(\frac{\%\ Period}{25}\right)+.973}\right],$$

while the lower bound F_2 is defined by

$$50\%\left[\frac{\%\ Period}{25}\right]^{1.5}.$$

As would be readily understood by those skilled in the art, the boundaries for the other quadrants defined by F_1 and F_2 as follows:

Quadrant I (-25% to 0% Period):
Lower bound = $-F_1$(-% Period),
Upper bound = $-F_2$(-% Period);
Quadrant III (25% to 50% Period):
Lower bound = F_2(50 - % Period),
Upper bound = F_1(50 - % Period); and
Quadrant IV (50% to 75% Period):
Lower bound = $-F_1$(% Period - 50)
Upper bound = $-F_2$(% Period - 50).

A more preferred profile range is indicated by the dashed lines indicated in FIG. 3. In quadrant II, this profile is defined by an upper bound F_3 and a lower bound F_4. The upper bound F_3 is defined in quadrant II by

$$100\%\left\lfloor \frac{\%\ Period}{25} \right\rfloor,$$

and the lower bound is defined in quadrant II by

$$100\%\left\lfloor \frac{\%\ Period}{25} \right\rfloor^{p}.$$

Accordingly, the other boundaries are given by:

Quadrant I (-25% to 0% Period):

Lower bound = $-F_3$(-% Period),

Upper bound = $-F_4$(-% Period);

Quadrant III (25% to 50% Period):

Lower bound = F_4(50 - % Period),

Upper bound = F_3(50 - % Period); and

Quadrant IV (50% to 75% Period):

Lower bound = $-F_3$(% Period - 50)

Upper bound = $-F_4$(% Period - 50).

As also shown in FIG. 2, the solid line P_1 of FIG. 3 illustrates the linear combination of a triangular waveform and its- cubic. More particularly, this profile is defined quadrant II by F_5 which is equal to

$$100\%[0.45(\%\ Period/25)^3 + 0.55(\%\ Period/25)].$$

Accordingly, the solid line is defined in the other quadrants as follows:

Quadrant I (-25% to 0% Period):

$-F_5$(-% Period);

Quadrant III (25% to 50% Period):

F_5(50 - % Period); and

Quadrant IV (50% to 75% Period):

$-F_5$(% Period - 50)

FIG. 5 illustrates yet another embodiment of a profile for the frequency deviation modulation which may be scaled to fit within the outermost profile defined by F_1 and F_2 as would be readily appreciated by those of skill in the art.

Referring now additionally to FIGS. 6 through 9, preferred circuit embodiments for the SSCG **14** are described. The block diagrams are similar to several conventional phase locked loop (PLL) frequency synthesizer chips; however, a modulation section is added which includes a programmable modulation generator in several embodiments, or an analog modulation generator in other embodiments. The modulation is fed into a voltage controlled oscillator (VCO) or oscillator tank circuit to give the desired modulation index.

The SSCG **14** may desirably be programmable via an I^2C serial bus or select lines to allow variation of the center frequency, maximum frequency deviation and modulation frequency. A single +5V supply, minimal external circuitry and a crystal will produce a TTL and CMOS compatible output with controlled rise and fall times. In addition, all inputs are standard TTL compatible.

The following electrical characteristics (TABLE 2) and switching characteristics (TABLE 3) given below are also desirably met by the embodiments of the SSCG **14** to be compatible with conventional digital circuits or microprocessors clock input requirements.

TABLE 2

- Electrical Characteristics					
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Load Capacitance	C_L	-	30	50	pF
Quiescent Supply Current	I_{CC}	-	-	45	mA

TABLE 3 - Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Output Rise (0.8 to 2.0V) and Fall Time (2.0V to 0.8V)	t_{TLH}, t_{THL}	1	2	3	ns
Maximum Frequency Deviation*	ΔF_{max}	0	100	250	KHz
Modulating Frequency*	F_{mod}	15	30	50	KHz

* Programmable via serial link.

Referring first to the schematic block diagram of FIG. 6, a phase locked loop (PLL) implementation of the SSCG indicated generally by reference numeral **30** according to the invention is first explained. Y1 **31** is a piezoelectric crystal used with an oscillator circuit **33** to generate a stable clock pulse train or unmodulated clock signal. A first programmable counter **35** divides the unmodulated clock signal by an integer number (M). A voltage controlled oscillator **39** (VCO) generates an output clock signal, output from a buffer **40**, that is proportional to the input voltage from the phase detector **37** and filter **38**.

A second programmable counter **42** divides the signal from the VCO **39** by an integer number (N). The phase detector **37** and filter **38** generate an analog signal that is proportional to the error in phase between first and second programmable counters **35, 42**, respectively. Accordingly, the clock signal output from the buffer **40** is equal to the oscillator frequency times N/M. As would be readily understood by those skilled in the art, when N and M are constant, this circuit operates as a standard (PLL) circuit.

The spread spectrum modulation according to the invention is introduced in this embodiment by the spread spectrum modulation means **41** which changes M and N as a function of time. A third programmable counter **45** divides the signal from the oscillator **33** by an integer number (I) which sets the rate that M and N change, or modulation frequency. First and second look-up tables **46, 47**, respectively, are the tabilized values for M and N which modulate the output clock signal frequency. An up/down counter **49** is used to index successive entries in the look-up tables. A serial link **51**, which is not required for operation, may be used to program different values in the programmable counters or look-up tables to modify modulation characteristics.

Referring now to FIG. 7, a second embodiment of the SSCG generally designated by reference numeral **50** is described. Elements previously discussed are indicated by like numerals and need not be described further. In this embodiment, the spread spectrum modulation is introduced by a second VCO **51** and an analog circuit **52**. The second VCO creates a clock signal identical to the first VCO **39** when no modulation is present. The second VCO **51** responds to the analog modulation to thereby create the spread spectrum clock output signal.

An embodiment of the analog modulation circuit **52** may include an oscillator to generate the modulation frequency, an integrator to generate a triangle wave function (r(t)), a log anti-log amplifier (alog(3log(r(t)))), and an adder to generate a modulation profile of .55r(t)+.45(alog(3log(r(t)))) as shown by plot P1 in FIG. 3. An alternative of the illustrated embodiment would be to add the modulation to the first VCO **39** input, as would be readily understood by those skilled in the art.

FIG. 8 illustrates yet another embodiment of the SSCG **70** according to the invention. An inverting amplifier **71** with an inductor L and a capacitor C1 forms a simple oscillator circuit **72** to generate a stable clock signal. Capacitors C1, C3 and varactor diode D are used to change the effective capacitance of C1 which will thereby change the oscillator circuit frequency. The varactor diode changes its junction capacitance proportional to the voltage applied thereacross. The analog modulation circuit **52** is preferably the same as discussed above with reference to FIG. 7. The output of the inverting amplifier **71** is a spread spectrum clock signal that can be used directly or that may also be scaled to any other frequency by adding a PLL circuit as illustrated. A first programmable counter **35** divides the oscillator signal by an integer number (M), while the VCO **39** generates a clock signal proportion to the input voltage from the phase detector **37** and filter **38**. The second programmable counter **42** divides the VCO signal by an integer number (N). The phase detector **37** and filter **38** output an analog signal that is proportional to the error in phase between the first and second programmable counters **35, 42**, respectively. The divide by 2 circuit **63** may be used to generate a clock output signal having a 50% duty cycle as would be readily understood by those skilled in the art.

Still another embodiment of an SSCG **80** is illustrated in FIG. 9 and is described as follows. The illustrated embodiment is similar to that shown in FIG. 7, but the modulation is created by a ROM **82** having stored therein modulation amplitude values that are fed into a digital to analog convertor **83** (DAC). An up/down counter **84** is used to index the values in the ROM **82** while a third programmable counter **85** sets the modulation frequency.

Another embodiment of an SSCG may include a direct digital synthesizer. A crystal and oscillator circuit generate a stable or unmodulated clock signal. As would be readily understood by those skilled in the art, the direct digital synthesizer (DDS) is an accumulator with a phase constant added to the accumulator every clock cycle and which in conjunction with a read only memory (ROM) produces a square wave from the Most Significant Bit (MSB). The frequency of an output square wave can be modulated by changing the phase constant as a function of time. This is preferably accomplished using a programmable up/down counter, and a look-up table similar to those illustrated in FIG. 6. A VCO generates a clock signal proportional to the input voltage from a phase detector and filter. A programmable counter divides the VCO signal by an integer number (N). The phase detector and filter also output an analog signal that is proportional to the error in phase between programmable counter and the DDS circuit. The spread spectrum modulated clock signal may be output from a divider or buffer.

As would be readily understood by those skilled in the art, in an implementation of any of the circuits described herein in a physical package, several such spread spectrum clock generating circuits (SSCG's) may be found in the same DIP. In addition, a standard phase locked loop frequency synthesizer may also be located in the same DIP to provide standard clock signals, if desired. The SSCG may also be included internally with a microprocessor or any other digital or analog circuit.

A method according to the invention is for generating the spread spectrum clock output signal. The method preferably includes the steps of: generating a series of clock pulses, and spread spectrum modulating the series of clock pulses to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced along with the series of clock pulses. The step of spread spectrum modulating the series of clock pulses preferably includes the step of frequency modulating the clock pulses with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period, as described in greater detail above.

The step of frequency modulating the series of clock pulses preferably includes modulating the series of clock pulses with a periodic waveform having a period of less than about 500 microseconds. The spread spectrum modulation according to the invention causes varying of the clock fundamental frequency, which in turn, may result in a 5-10% reduction in average clock frequency compared to the fixed frequency of a conventional clock circuit. However, for a significant number of applications, the SSCG according to the invention significantly reduces measured EMI emissions without adversely affecting overall electronic device performance.

Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the invention is not to be limited to the specific embodiments disclosed, but is defined by the scope of the appended claims.

Claims

1. A clock circuit for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said clock circuit comprising:

   oscillator means for generating a reference frequency signal; and

   spread spectrum clock generating means cooperating with said oscillator means for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency.

2. A clock circuit according to Claim 1 wherein said spread spectrum clock generating means comprises:

   clock pulse generating means for generating a series of generally rectangularly shaped electrical clock pulses; and

   spread spectrum modulating means cooperating with said clock pulse generating means for modulating same to broaden and flatten amplitudes of impulse-shaped EMI spectral components which would otherwise be produced by said clock pulse generating means.

3. A clock circuit according to Claim 2 wherein said spread spectrum modulating means comprises frequency modulating means for frequency modulating said clock pulse generating means.

4. A clock circuit according to Claim 3 wherein said frequency modulating means comprises profile modulating means for frequency modulating said clock pulse generating means with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period.

5. A clock circuit according to Claim 3 wherein said frequency modulating means comprises profile modulating means for modulating the clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein said predetermined upper bound is defined in a second quadrant of 0 to 25% Period by F_1 which is equal to

$$100\%\left[-1+\sqrt{-\left(\frac{\%\ Period}{25}\right)^2+4\left(\frac{\%\ Period}{25}\right)+.973}\right],$$

wherein said predetermined lower bound over the second quadrant is defined by F_2 which is equal to

$$50\%\left[\frac{\%\ Period}{25}\right]^{10};$$

wherein for a first quadrant between -25% to 0% Period the lower bound is equal to $-F_1$(-% Period) and the upper bound is equal to $-F_2$(-% Period); wherein for a third quadrant between 25% to 50% Period the lower bound is equal to F_2(50 - % Period), and the upper bound is equal to F_1(50 - % Period); and wherein for a fourth quadrant the lower bound is equal to $-F_1$(% Period - 50) and the upper bound is equal to $-F_2$(% Period - 50).

6. A clock circuit according to Claim 3 wherein said frequency modulating means comprises profile modulating means for modulating the clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein said predetermined upper bound for a second quadrant is defined by F_3 which is equal to

$$100\%\left|\frac{\%\ Period}{25}\right|,$$

wherein said predetermined lower bound is defined by F_4 which is equal to

$$100\%\left[\frac{\%\ Period}{25}\right]^3;$$

wherein for a first quadrant between -25% to 0% Period the lower bound is equal to $-F_3$(-% Period) and the upper bound is equal to $-F_4$(-% Period); wherein for a third quadrant between 25% to 50% Period the lower bound is equal to F_4(50 - % Period), and the upper bound is equal to F_3(50 - % Period); and wherein for a fourth quadrant the lower bound is equal to $-F_3$(% Period - 50) and the upper bound is equal to $-F_4$(% Period - 50).

7. A clock circuit according to Claim 3 wherein said frequency modulating means comprises profile modulating means for modulating said clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a second quadrant by F_5 which is equal to

$$100\%[0.45(\%\ Period/25)^3 + 0.55(\%\ Period/25)];$$

wherein for a first quadrant between -25% to 0% Period the profile is equal to $-F_5$(-% Period); wherein for a third quadrant between 25% to 50% Period the profile is equal to F_5(50 - % Period); and wherein for a fourth quadrant the profile is equal to $-F_5$(% Period - 50).

8. A clock circuit according to any of claims 3 to 7 wherein said clock pulse generating means comprises a phase locked loop.

9. A clock circuit according to Claim 8 wherein said frequency modulating means comprises an analog mod-

ulating generator operatively connected to said phase locked loop.

10. A clock circuit according to Claim 8 wherein said frequency modulating means comprises a programmable modulating generator operatively connected to said phase locked loop.

11. A clock circuit according to any of claims 3 to 10 wherein said frequency modulating means comprises means for modulating said clock pulse generating means with a periodic waveform having a period of less than about 500 microseconds.

12. A clock circuit according to any preceding claim wherein said oscillator means comprises a crystal having a predetermined resonant frequency.

13. A clock circuit for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said clock circuit comprising:

oscillator means for generating a reference frequency signal; and

spread spectrum clock generating means cooperating with said oscillator means for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency, said spread spectrum clock generating means comprising

clock pulse generating means for generating a series of clock pulses, and

profile modulating means for frequency modulating the clock pulse generating means with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period.

14. A clock circuit according to Claim 13 wherein said profile modulating means comprises means for modulating the clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein said predetermined upper bound is defined in a second quadrant of 0 to 25% Period by F_1 which is equal to

$$100\%\left[-1+\sqrt{-\left(\frac{\%\ Period}{25}\right)^2-4\left(\frac{\%\ Period}{25}\right)+.973}\right],$$

wherein said predetermined lower bound over the second quadrant is defined by F_2 which is equal to

$$50\%\left[\frac{\%\ Period}{25}\right]^{10};$$

wherein for a first quadrant between -25% to 0% Period the lower bound is equal to $-F_1$(-% Period) and the upper bound is equal to $-F_2$(-% Period); wherein for a third quadrant between 25% to 50% Period the lower bound is equal to F_2(50 - % Period), and the upper bound is equal to F_1(50 - % Period); and wherein for a fourth quadrant the lower bound is equal to $-F_1$(% Period - 50) and the upper bound is equal to $-F_2$(% Period - 50).

15. A clock circuit according to Claim 13 wherein said profile modulating means comprises means for modulating the clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein said predetermined upper bound for a second quadrant is defined by F_3 which is equal to

$$100\%\left|\frac{\%\ Period}{25}\right|,$$

wherein said predetermined lower bound is defined by F_4 which is equal to

$$100\%\left[\frac{\%\ Period}{25}\right]^3;$$

wherein for a first quadrant between -25% to 0% Period the lower bound is equal to $-F_3$(-% Period) and the upper bound is equal to $-F_4$(-% Period); wherein for a third quadrant between 25% to 50% Period the lower bound is equal to F_4(50 - % Period), and the upper bound is equal to F_3(50 - % Period); and wherein for a fourth quadrant the lower bound is equal to $-F_3$(% Period - 50) and the upper bound is equal to $-F_4$(% Period - 50).

16. A clock circuit according to Claim 13 wherein said profile modulating means includes means for modulating said clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a second quadrant by F_5 which is equal to

$$100\%[0.45(\%\ Period/25)^3 + 0.55(\%\ Period/25)];$$

wherein for a first quadrant between -25% to 0% Period the profile is equal to $-F_5$ (-% Period); wherein for a third quadrant between 25% to 50% Period the profile is equal to F_5(50 - % Period); and wherein for a fourth quadrant the profile is equal to $-F_5$(% Period - 50).

17. A clock circuit according to any of claims 13 to 16 wherein said clock pulse generating means comprises a phase locked loop.

18. A clock circuit according to Claim 17 wherein said profile modulating means comprises an analog modulating generator operatively connected to said phase locked loop.

19. A clock circuit according to Claim 17 wherein said profile modulating means comprises a programmable modulating generator operatively connected to said phase locked loop.

20. A clock circuit according to any of claims 13 to 19 wherein said profile modulating means comprises means for modulating said clock pulse generating means with the periodic waveform having a period of less than about 500 microseconds.

21. A clock circuit according to any of claims 13 to 20 wherein said oscillator means comprises a crystal having a predetermined resonant frequency.

22. A clock circuit for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said clock circuit comprising:

clock pulse generating means for generating a series of clock pulses; and

spread spectrum modulating means cooperating with said clock pulse generating means for modulating same to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced by said clock pulse generating means.

23. A clock circuit according to claim 22 and as claimed in any of claims 3 to 12.

24. An electronic device having reduced amplitude electromagnetic interference (EMI) spectral components, said electronic device comprising:

spread spectrum clock generating means for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency; and

a digital circuit connected to said spread spectrum clock generating means and having a clock input driven by the spread spectrum clock output signal.

25. An electronic device according to Claim 24 wherein said spread spectrum clock generating means comprises:

clock pulse generating means for generating a series of clock pulses; and

spread spectrum modulating means cooperating with said clock pulse. generating means for modulating same to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced by said clock pulse generating means.

26. An electronic device according to claim 25 and including the features of any of claims 3 to 12.

27. A method for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said method comprising the step of generating a spread spectrum clock output signal so that the spread spectrum clock output signal has a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency.

28. A method according to Claim 27 wherein the step of generating the spread spectrum clock output signal comprises the steps of:

generating a series of clock pulses; and

spread spectrum modulating the series of clock pulses to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced along with the series of clock pulses.

29. A method according to Claim 28 wherein the step of spread spectrum modulating comprises frequency modulating the series of clock pulses.

30. A method according to Claim 29 wherein the step of frequency modulating comprises modulating the series of clock pulses with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period.

31. A method according to Claim 29 wherein the step of frequency modulating comprises modulating the series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein the predetermined upper bound is defined in a second quadrant of 0 to 25% Period by F_1 which is equal to

$$100\%\left[-1+\sqrt{-\left(\frac{\%\ Period}{25}\right)^2+4\left(\frac{\%\ Period}{25}\right)+.973}\right],$$

wherein the predetermined lower bound over the second quadrant is defined by F_2 which is equal to

$$50\%\left[\frac{\%\ Period}{25}\right]^{10};$$

wherein for a first quadrant between -25% to 0% Period the lower bound is equal to $-F_1$(-% Period) and the upper bound is equal to $-F_2$(-% Period); wherein for a third quadrant between 25% to 50% Period the lower bound is equal to F_2(50 - % Period), and the upper bound is equal to F_1(50 - % Period); and wherein for a fourth quadrant the lower bound is equal to $-F_1$(% Period - 50) and the upper bound is equal to $-F_2$(% Period - 50).

32. A method according to Claim 29 wherein the step of frequency modulating comprises modulating the series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein the predetermined upper bound for a second quadrant is defined by F_3 which is equal to

$$100\%\left[\frac{\%\ Period}{25}\right],$$

wherein the predetermined lower bound is defined by F_4 which is equal to

$$100\%\left[\frac{\%\ Period}{25}\right]^3;$$

wherein for a first quadrant between -25% to 0% Period the lower bound is equal to $-F_3(-\%\ \text{Period})$ and the upper bound is equal to $-F_4(-\%\ \text{Period})$; wherein for a third quadrant between 25% to 50% Period the lower bound is equal to $F_4(50 - \%\ \text{Period})$, and the upper bound is equal to $F_3(50 - \%\ \text{Period})$; and wherein for a fourth quadrant the lower bound is equal to $-F_3(\%\ \text{Period} - 50)$ and the upper bound is equal to $-F_4(\%\ \text{Period} - 50)$.

33. A method according to Claim 29 wherein the step of frequency modulating comprises modulating the series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a second quadrant by F_5 which is equal to

$$100\%[0.45(\%\ \text{Period}/25)^3 + 0.55(\%\ \text{Period}/25)];$$

wherein for a first quadrant between -25% to 0% Period the profile is equal to $-F_5(-\%\ \text{Period})$; wherein for a third quadrant between 25% to 50% Period the profile is equal to $F_5(50 - \%\ \text{Period})$; and wherein for a fourth quadrant the profile is equal to $-F_5(\%\ \text{Period} - 50)$.

34. A method according to any of claims 29 to 33 wherein the step of frequency modulating comprises modulating the series of clock pulses with a periodic waveform having a period of less than about 500 microseconds.

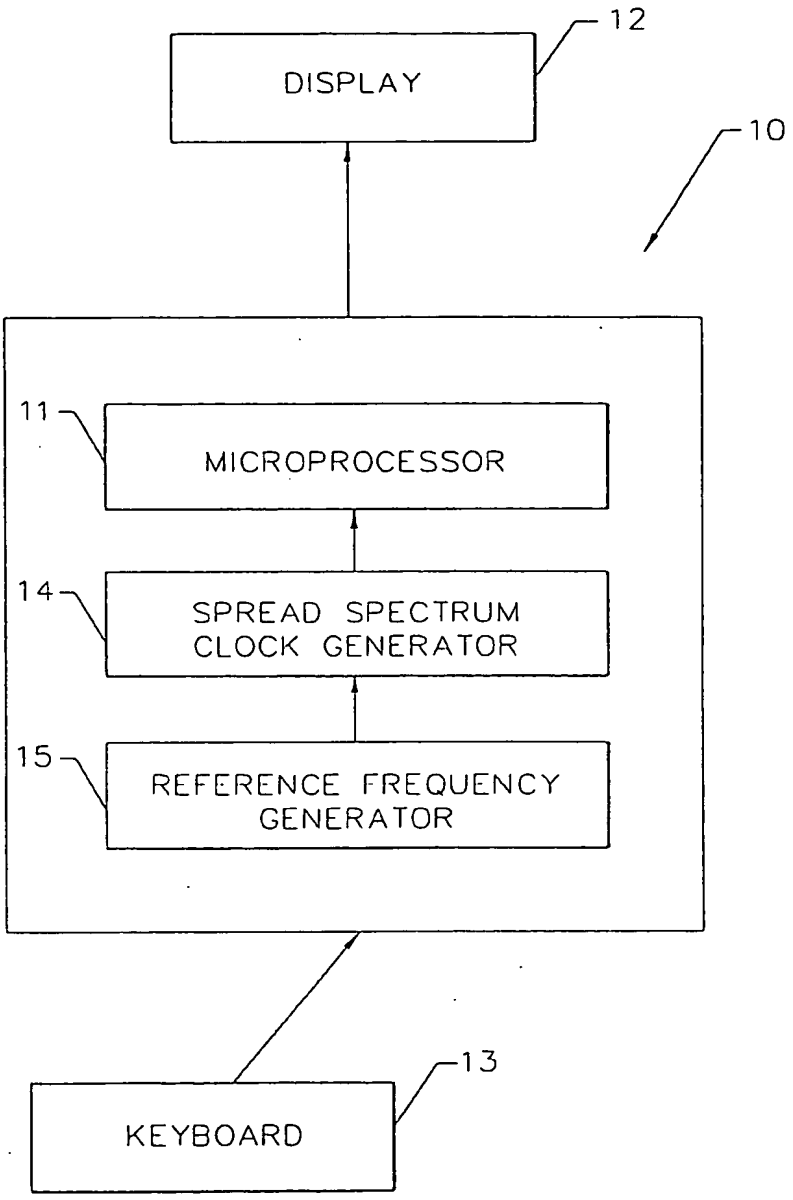
12
DISPLAY
10
11
MICROPROCESSOR
14
SPREAD SPECTRUM
CLOCK GENERATOR
15
REFERENCE FREQUENCY
GENERATOR
13
KEYBOARD

FIG. 1.

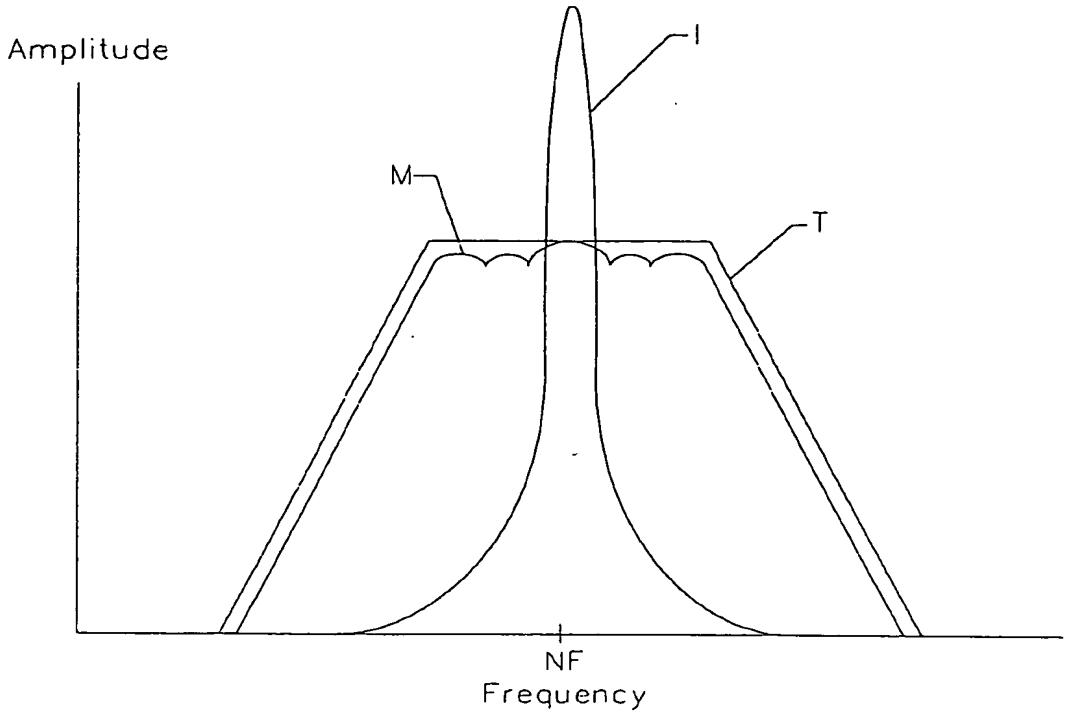
Amplitude
I
M
T
NF
Frequency

FIG. 2.

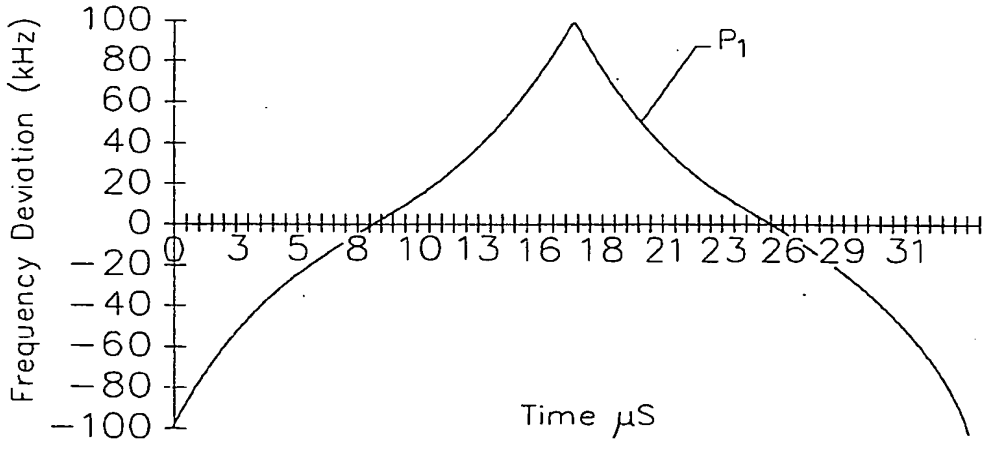
Frequency Deviation (kHz)
100
80
60
40
20
0
−20
−40
−60
−80
−100
0 3 5 8 10 13 16 18 21 23 26 29 31
P1
Time μS

FIG. 3.

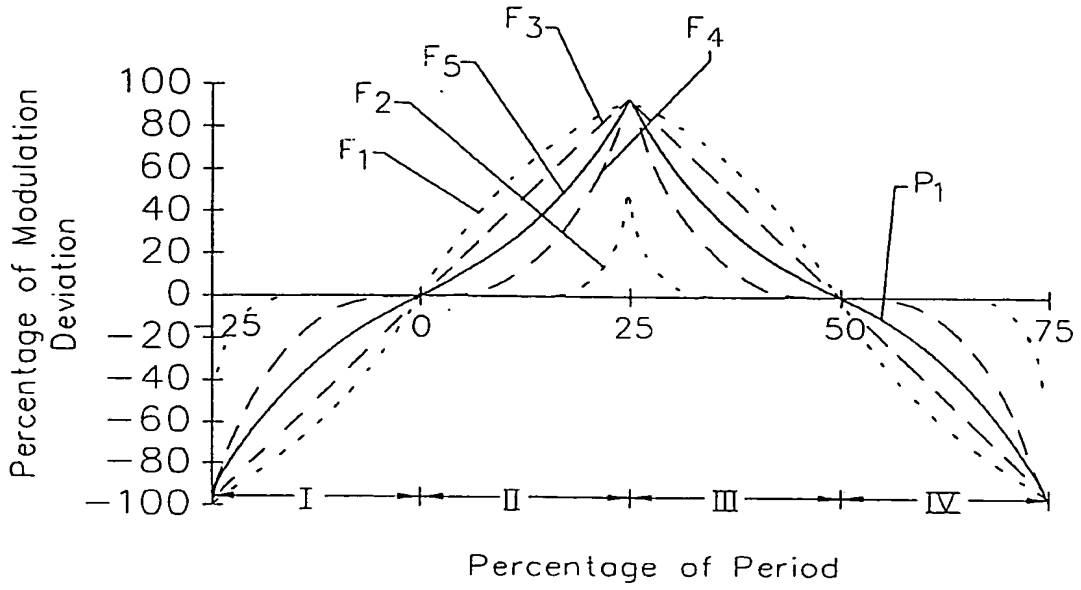
F3
F4
F5
F2
F1
P1
100
80
60
40
20
0
−20
−40
−60
−80
−100
25
0
25
50
75
I
II
III
IV
Percentage of Modulation Deviation
Percentage of Period

FIG. 4.

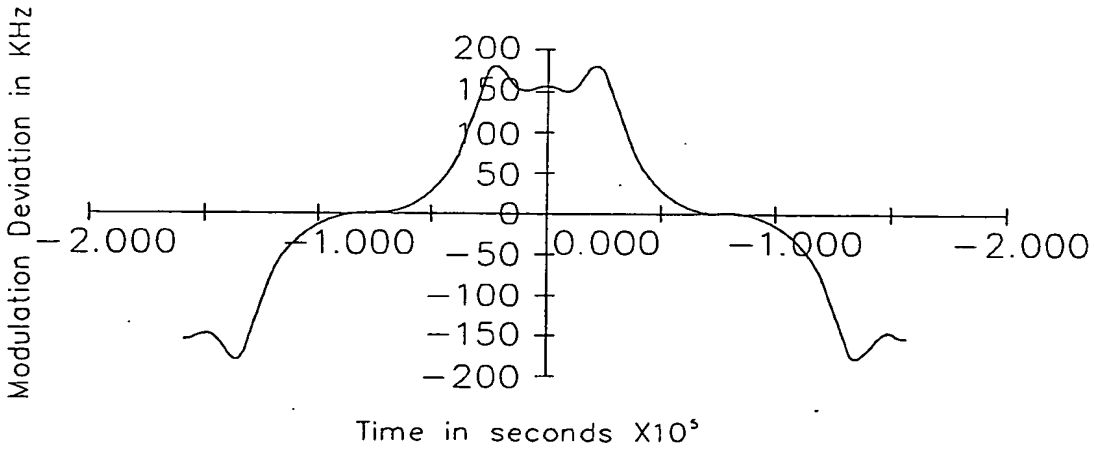
200
150
100
50
0
−50
−100
−150
−200
−2.000
−1.000
0.000
−1.000
−2.000
Modulation Deviation in KHz
Time in seconds X10⁵

FIG. 5.

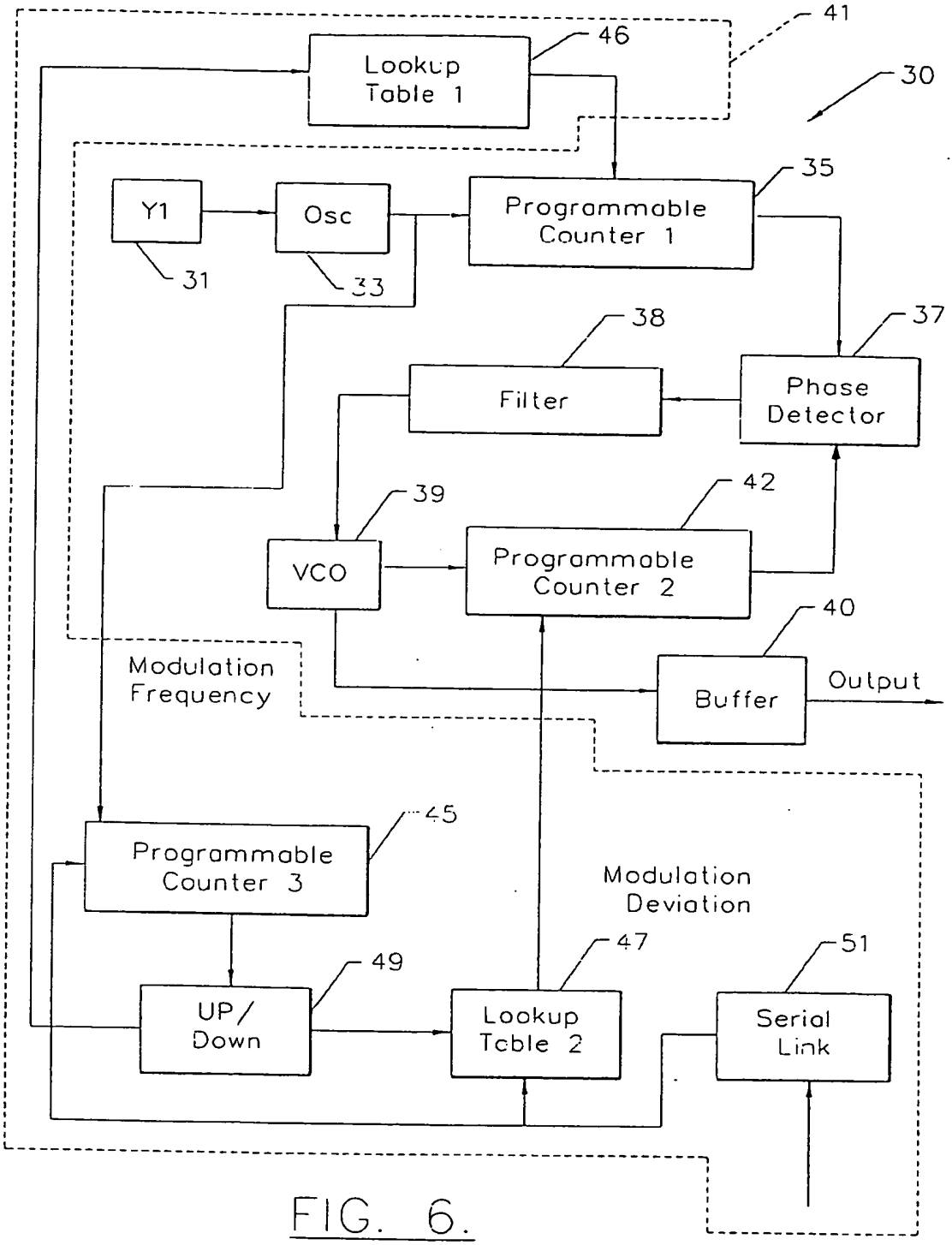
41
46
Lookup Table 1
30
35
Y1
Osc
Programmable Counter 1
31
33
38
37
Filter
Phase Detector
39
42
VCO
Programmable Counter 2
40
Modulation Frequency
Buffer
Output
45
Programmable Counter 3
Modulation Deviation
49
47
51
UP/ Down
Lookup Table 2
Serial Link

FIG. 6.

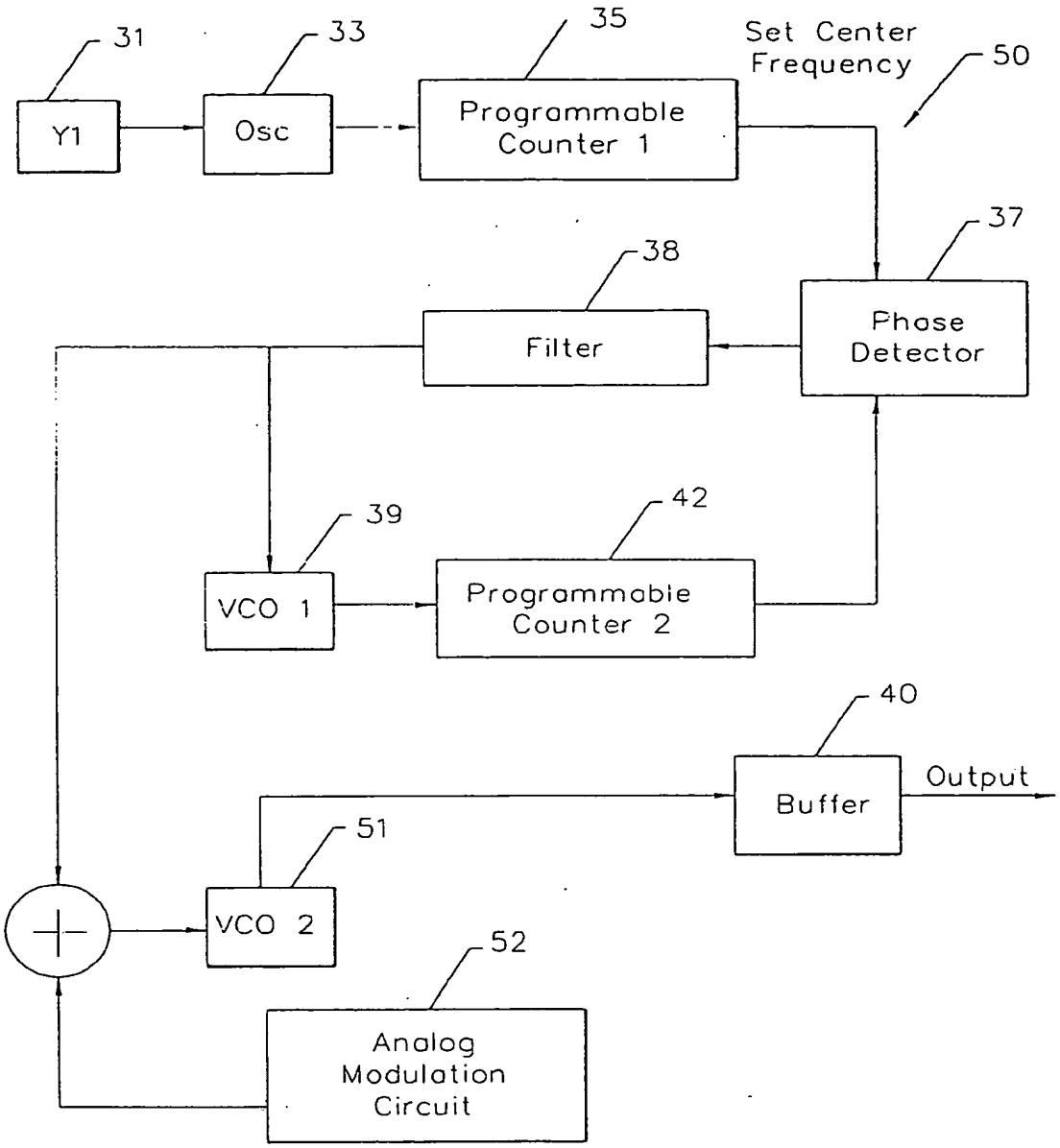
31
33
35
Set Center Frequency
50
Y1
Osc
Programmable Counter 1
37
38
Filter
Phase Detector
39
42
VCO 1
Programmable Counter 2
40
Buffer
Output
51
VCO 2
52
Analog Modulation Circuit

FIG. 7.

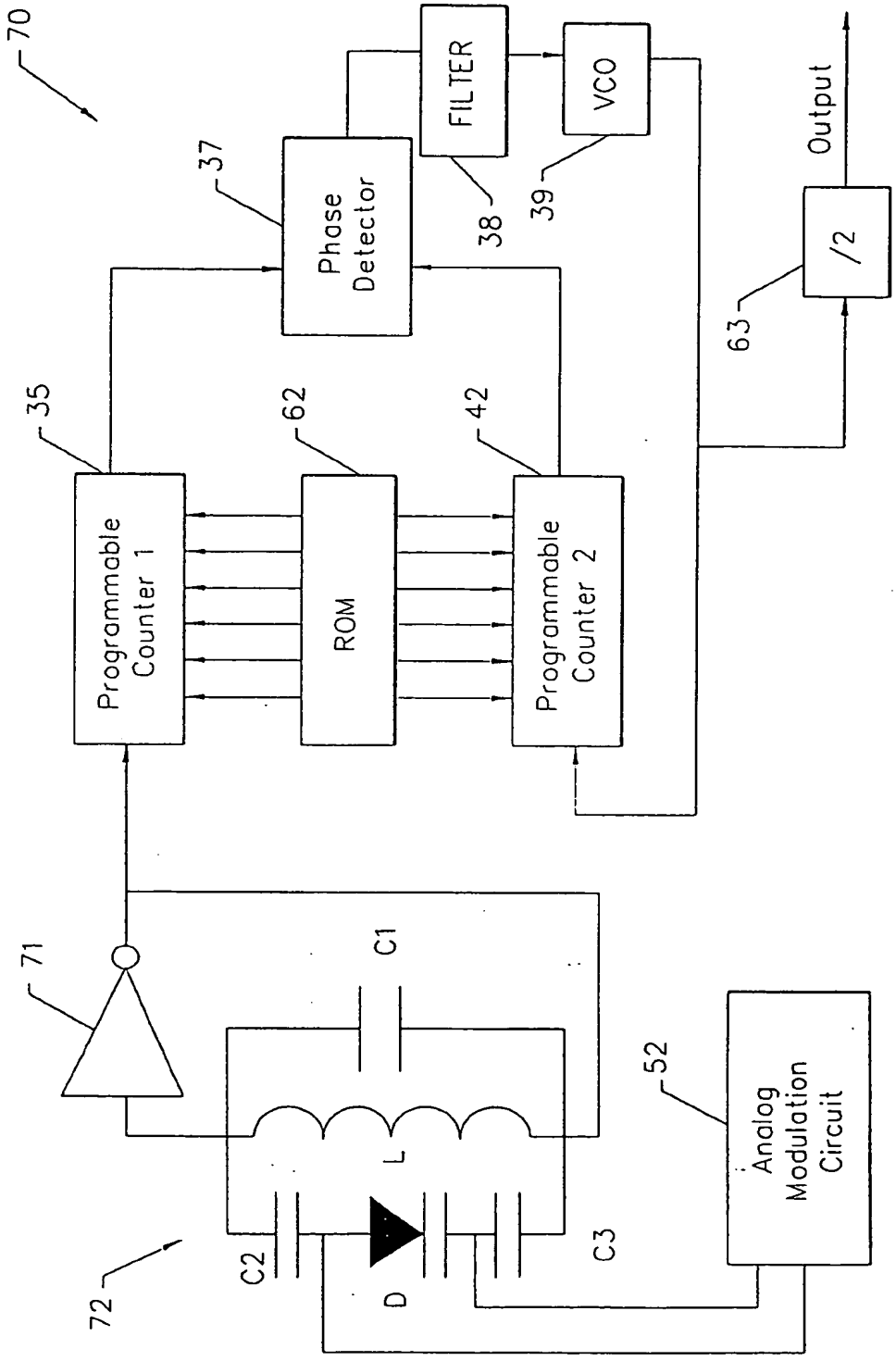
70
FILTER
VCO
Output
37
Phase Detector
38
39
/2
63
35
62
42
Programmable Counter 1
ROM
Programmable Counter 2
71
C1
52
Analog Modulation Circuit
L
C2
C3
D
72

FIG. 8.

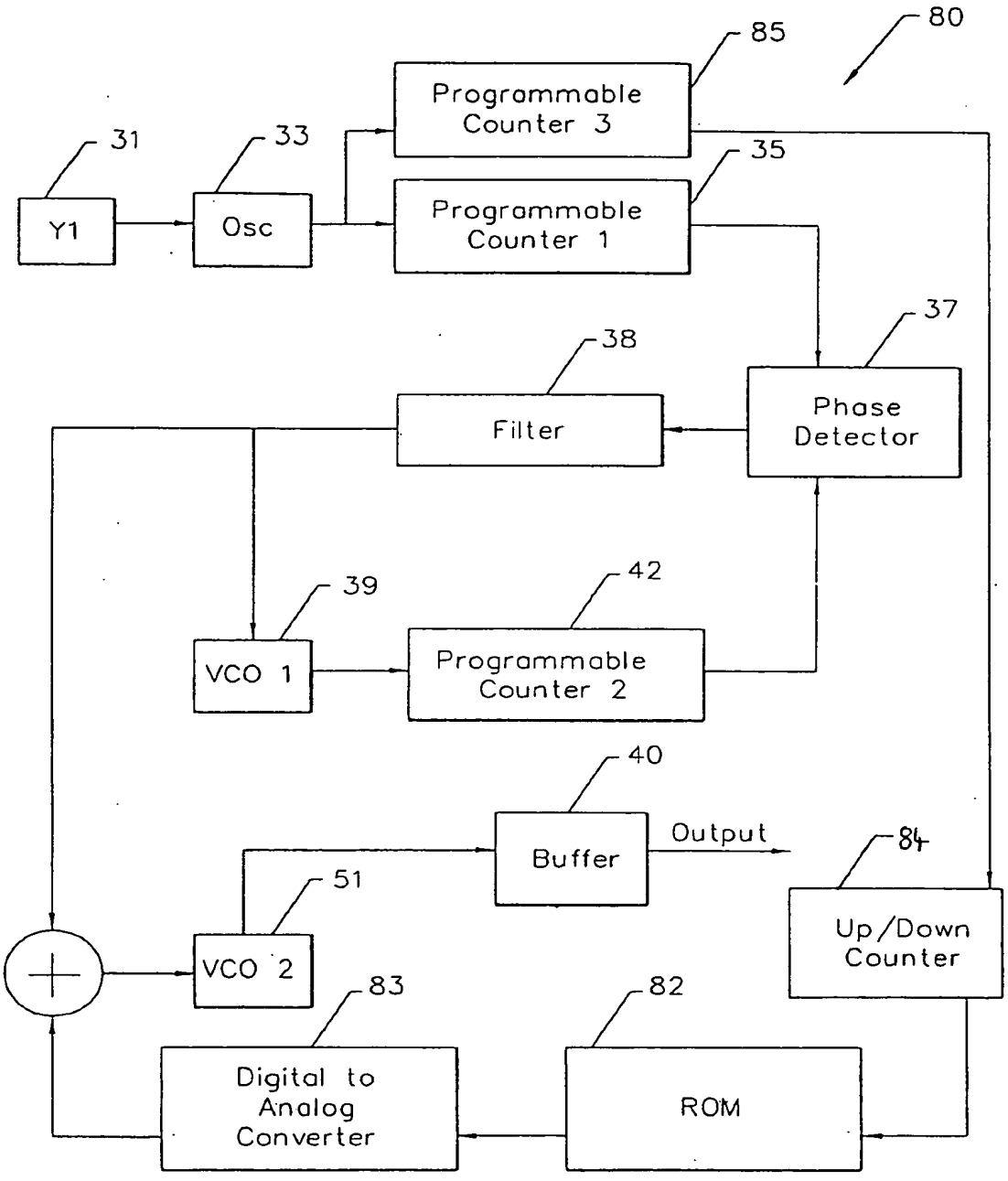
80
85
Programmable Counter 3
31
33
35
Y1
Osc
Programmable Counter 1
37
38
Filter
Phase Detector
39
42
VCO 1
Programmable Counter 2
40
Buffer
Output
84
51
Up/Down Counter
VCO 2
83
82
Digital to Analog Converter
ROM

FIG. 9.

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 8802

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	GB-A-2 128 828 (PRINTRONIX INC.)	1-3,8,9, 12,22, 27-29	H03C3/09 H03B29/00
A	* page 3, line 46 - line 79 *	13,17, 18,21, 24,25	
X	EP-A-0 163 313 (TEKTRONIX, INC.)	1-3,8,9, 12,22, 27-29	
A	* abstract; figure 1 *	13,17, 18,21, 24,25	
X	US-A-5 263 055 (CAHILL)	1-3,22, 27-29	
A	* the whole document *	13,24,25	
X	WO-A-90 14710 (MOTOROLA, INC.)	1-3,22, 27-29	
A	* the whole document *	13,24,25	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	BE-A-671 928 (WESTERN ELECTRIC COMPANY, INCORPORATED)		H03C H03B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13 March 1995	Peeters, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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